multiLane

ML4066-ANA Manual

Innovation for the next generation

multiLane

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1. Overview

The ML4066 is an Adaptor with diagnostic interface for the power, I2C and management interface control and alarm signals. The SFF analyzer board is connected to the ML4066 to enable live diagnosis for the transceiver and host.

2. SFF Analyzer

2.1 The SFF Analyzer features

- USB Interface
- Windows based GUI and API Library
- Detection and measurement of host pull up + pull down resistors on low speed signals
- Host VCC rails sampling measurement
- VCC spectral noise analysis
- I2C Analyzer
    - Bus Speed
    - ACK/ NACK Detection
    - Clock Stretching Analysis
    - Time Event Logging
- Functional tests
    - Control signals
    - Configuration registers
    - Ability to emulate optical module by loading identification registers with custom data
    - I2C Terminated by microcontroller, I2C slave compliant with MSA
    - Implements MSA Memory map and programmable new pages
    - Memory map can be loaded to replicate optical module's identification registers
    - Ability to control/monitor all low speed signals
    - Hot pluggable
- Alarm generation

2.2 SFF Analyzer GUI

2.2.1 VCC tab

The VCC tab allows the measurement of the VCCTX, RX and VCC1. The user should select the number of samples that will be multiplied by the sampling period selected from the Combobox. The default value of this period is 0.55µs.

The user can add two markers to the graph using the mouse right-click. To add other markers the user shall Clear all markers and add others.

The values of the markers and their difference are shown under the graph.

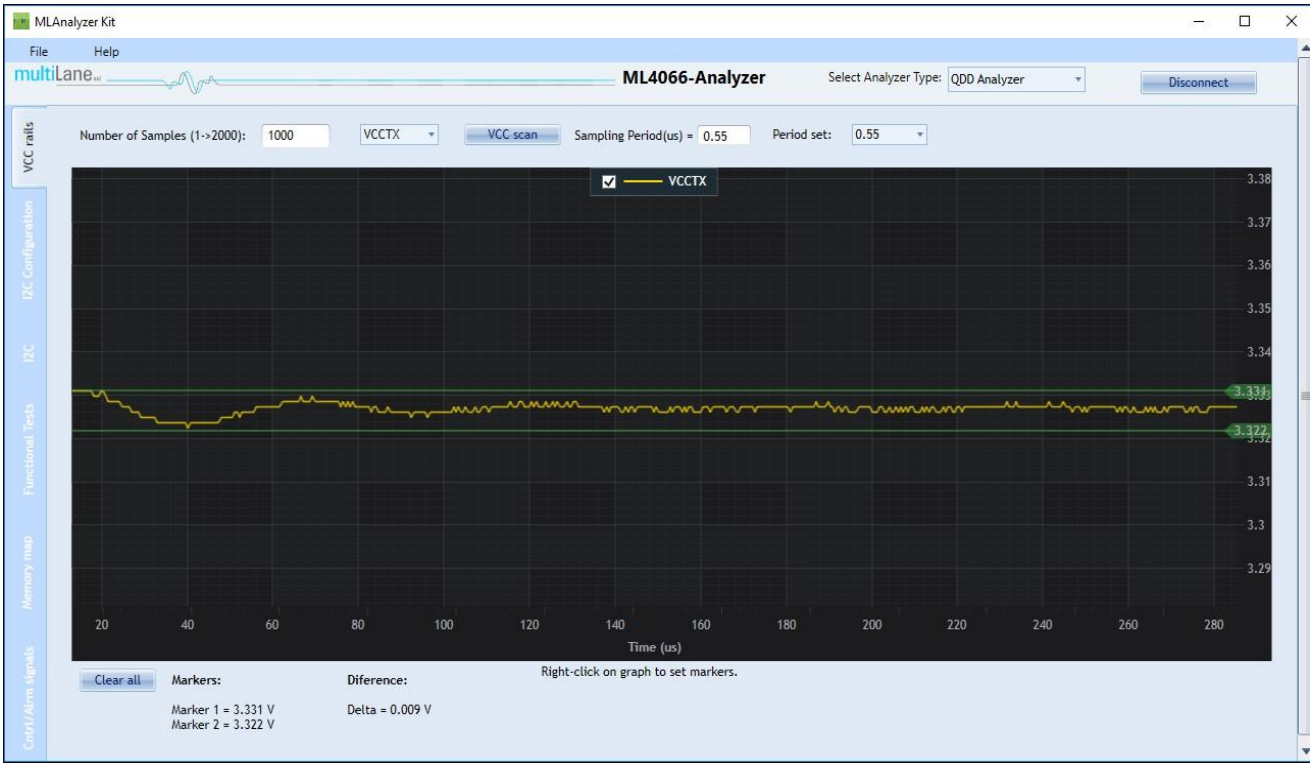
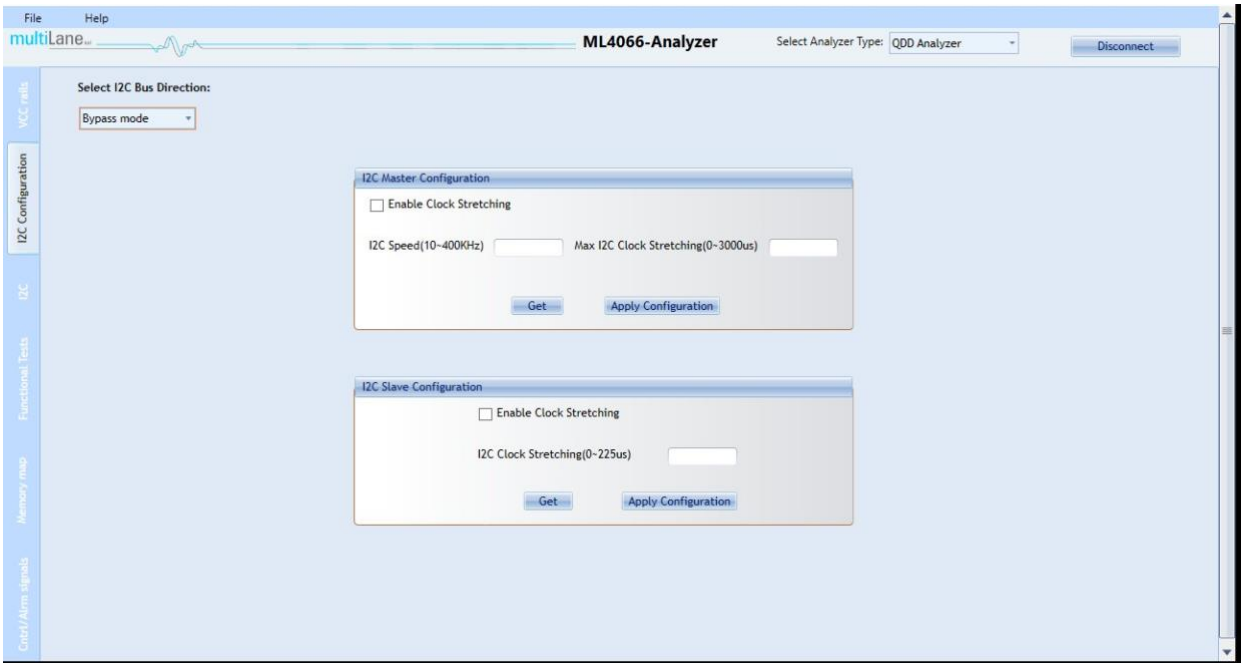


Figure 1: VCC tab

2.2.2 I2C Configuration Tab

This tab allows the user to manually configure the I2C bus direction, speed, and clock stretching.



When choosing **Internal Slave**, the user can Read/Write the Data of the Analyzer's EEPROM**. Internal Master** allows User to read/write on the Module.

Bypass mode makes the communication direct between the module and the host.

For the I2C Master configuration, use the Get button to retrieve the configuration. To change it, write the desired configuration then click "Apply Configuration". The max clock stretching corresponds to the maximum time that the Master waits for the slave's response. To set the max clock stretching the "Enable Clock Stretching" checkbox must be checked.

For I2C slave configuration, user can choose to enable/disable clock stretching, and can also set the clock stretching time that will be forced on SCL during I2C transactions

2.2.3 I2C tab

This tab analyzes the I2C packets. The graph will show the clock (SCL) and the data (SDA). The SCL rising edges are detected and the SDA values are shown at each rising edge (cf. image below). A vertical line is drawn at each rising edge and the SDA binary values are shown under the yellow SDA curve.

Figure 2: I2C tab

The image above refers to the I2C read command. The data packets are shown in a list under the graph.

The user can select the packet that he needs to visualize on the graph and it will show the range of that packet.

Each packet is delimited on the graph by the Start (marked in green) and Stop (marked in red) conditions (cf. image above).
Note that the user can show/hide any of the lines by clicking on the corresponding checkbox at the top of the graph.

The user can also change the sampling period using the combo box. This period will be multiplied by the number of samples chosen. Its default value is 0.963µs.

Note that for the reading process the user should select a higher number of samples so it can capture the whole packet.

Figure 3 - I2C Write

As for the description of the packet, each packet starts with the slave address A0 followed by the acknowledgment 0. The data afterword is the Data Word (7F is the page selection and 00 is the MemPage needed to write on). The second packet presents the writing process on the address 00(hex).

The free run checkbox is used to monitor the I2C bus. When checked, the monitoring function will start sampling directly after the I2C button is clicked.

When unchecked, the monitoring function will automatically detect I2C start frame.

2.2.4 Functional Tests tab

The functional tests tab gives access to the memory pages. The user can read/write on registers via I2C using this tab. To read/write from the module the user should select the “Internal Master” bus direction from the I2C configuration tab, or the “Internal Slave” to read/write from the EEPROM.

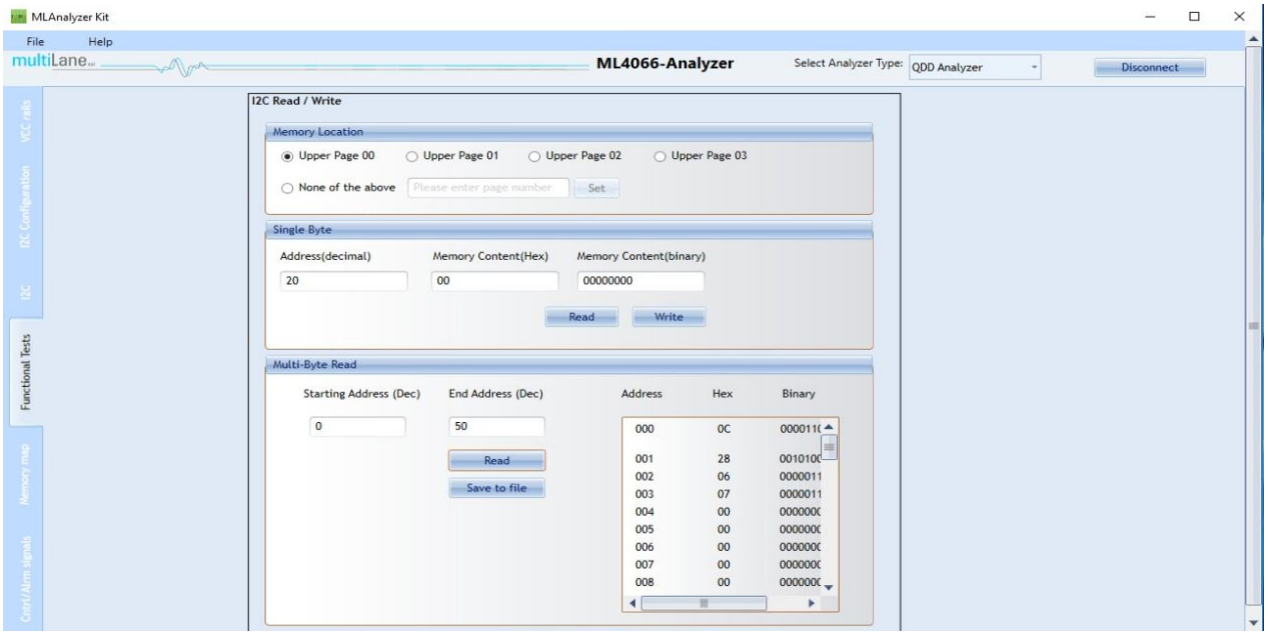


Figure 4: Functional Tests tab

For the SFP-Analyzer, the functional tests tab adds the slave addresses corresponding to the SFP standards.

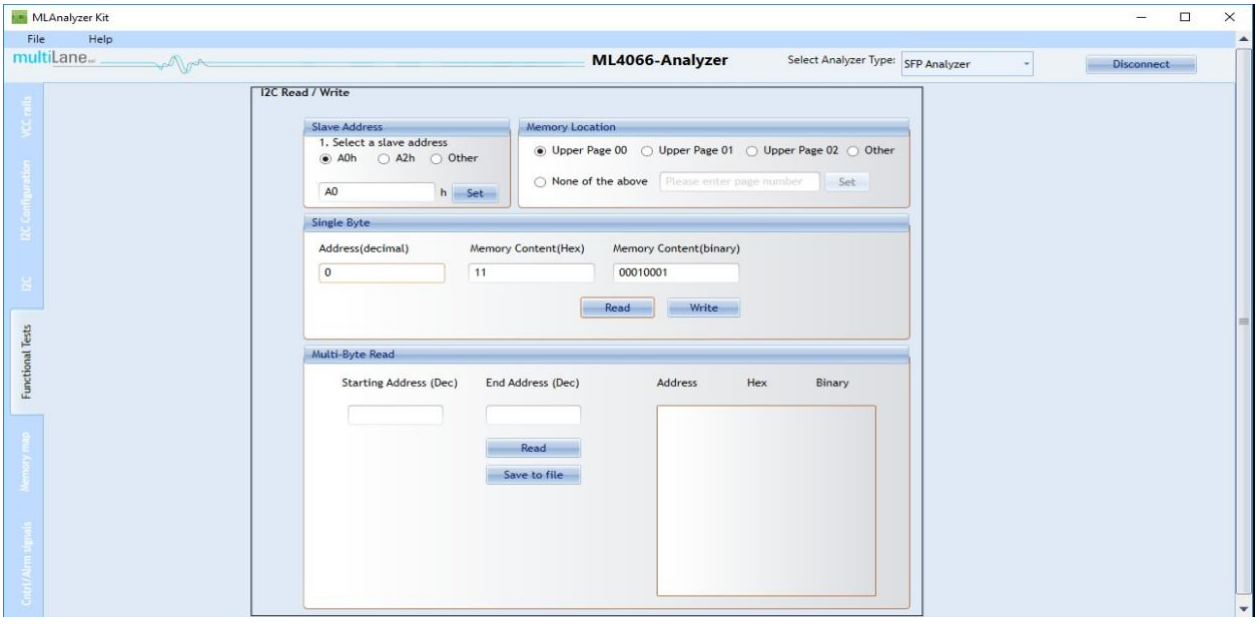


Figure 5-Functional Tests Tab for SFP-Analyzer

I2C Read/Write:

1. First, the user selects which page in the **Memory Location** he needs to perform a read or write operation on.
2. Then, he can use the **Single Byte** window to read/write one byte from the memory.
    a. Address: The address to read/write from.
    b. Memory Content: The data value to be read/written to the selected address (In Hex or in Binary)
3. Or, the user can use the **Multi-byte Read** to read/write multiple bytes between a Starting Address and an End Address that he specifies.

2.2.5 Memory Map tab

This tab gives access to the memory map of the module. It can be loaded to replicate optical module's identification registers.

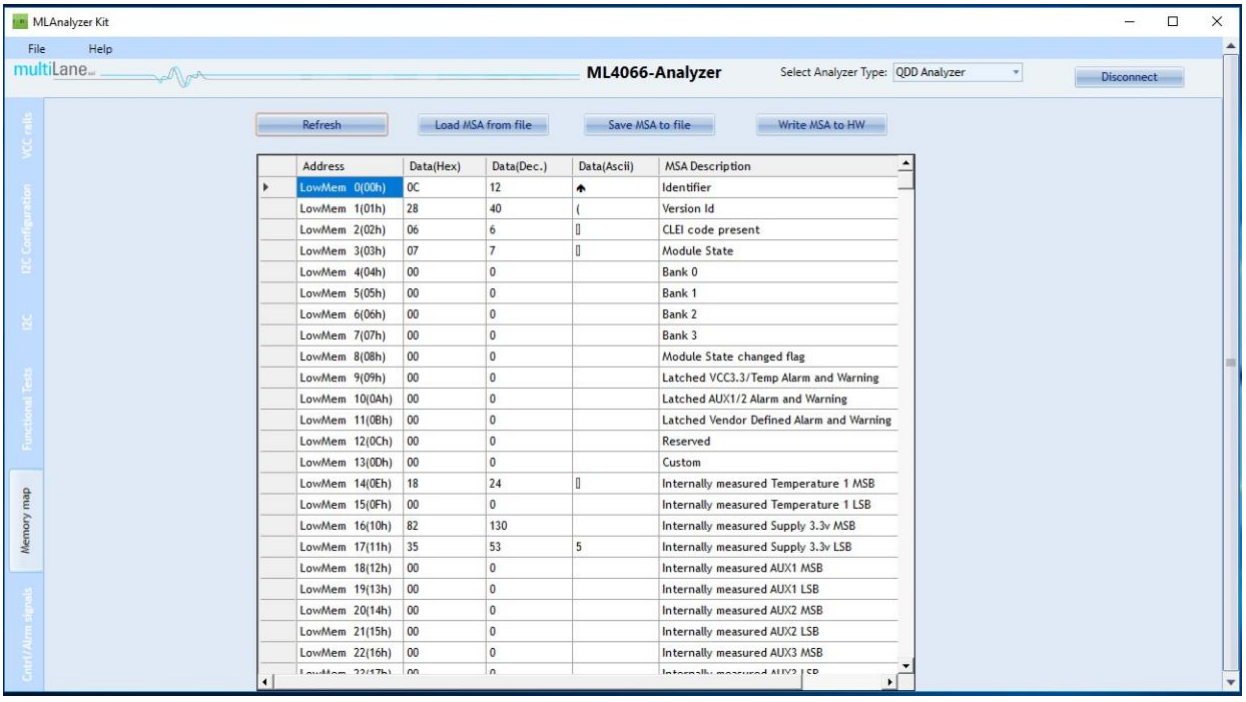


Figure 6: Memory Map tab

This screen allows User to Load or Save his custom MSA configuration.

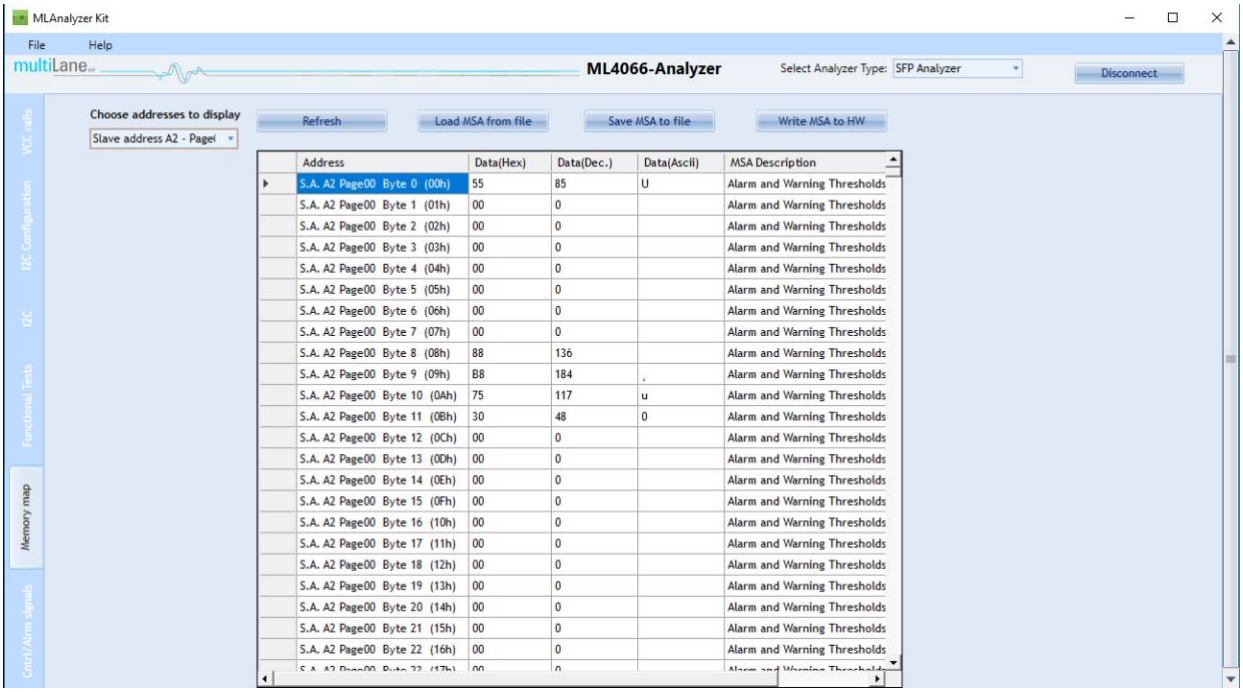
Data is displayed according to the selected I2C Bus Direction in a grid showing: register address, hex value, Decimal Values, ASCII value, MSA description.

- **Refresh** button: Read MSA Registers, and refresh values.
- **Write MSA to HW** button: Write the current MSA configuration to OSFP module.

- **Save MSA to file** button: Saves the current MSA memory to a file using Comma separated values (CSV) format.
- **Load MSA from file** button: Loads MSA values from file and map it to MSA memory.

When choosing **Internal Slave**, the user can Read/Write the Data of the Analyzer's EEPROM**. Internal Master** allows User to read/write on the Module. **Bypass mode** makes the communication direct between the module and the host.

For the SFP-Analyzer, the user can choose which slave address he wants and from which page he wants to read.



2.2.6 CNTRL/ALRM Signals tab

This tab allows detection and measurement of host pull up resistors on low speed signals and the detection of their state (either digital or analog). The user can also drive these signals using the corresponding checkboxes.

- Pull-Up Resistors window: The analyzer detects if the pull-up resistor of each signal is missing or not and it calculates its value. The range between 1.3KΩ and 10KΩ is acceptable indicating that a pull-up resistor is present. Below 1.3KΩ the resistor value is too low and you risk to have a "Short circuit". Above 10KΩ you risk of an "open circuit" case. The marge of accuracy for the resistor's value is about 1KΩ.
- For each signal the desired mode "Drive", "Bypass" or "Analog Sampler" is chosen. The Analog Monitor button displays the voltage of the desired signal. To manually assert/de-assert the signals, the "Drive" option must be chosen to be able to toggle the signal's checkbox. Finally, if "Bypass" mode is selected, the user can control the module externally and gets its status when the Get button is clicked.
- The Refresh button gets the initial states of the signals in "Drive" mode.

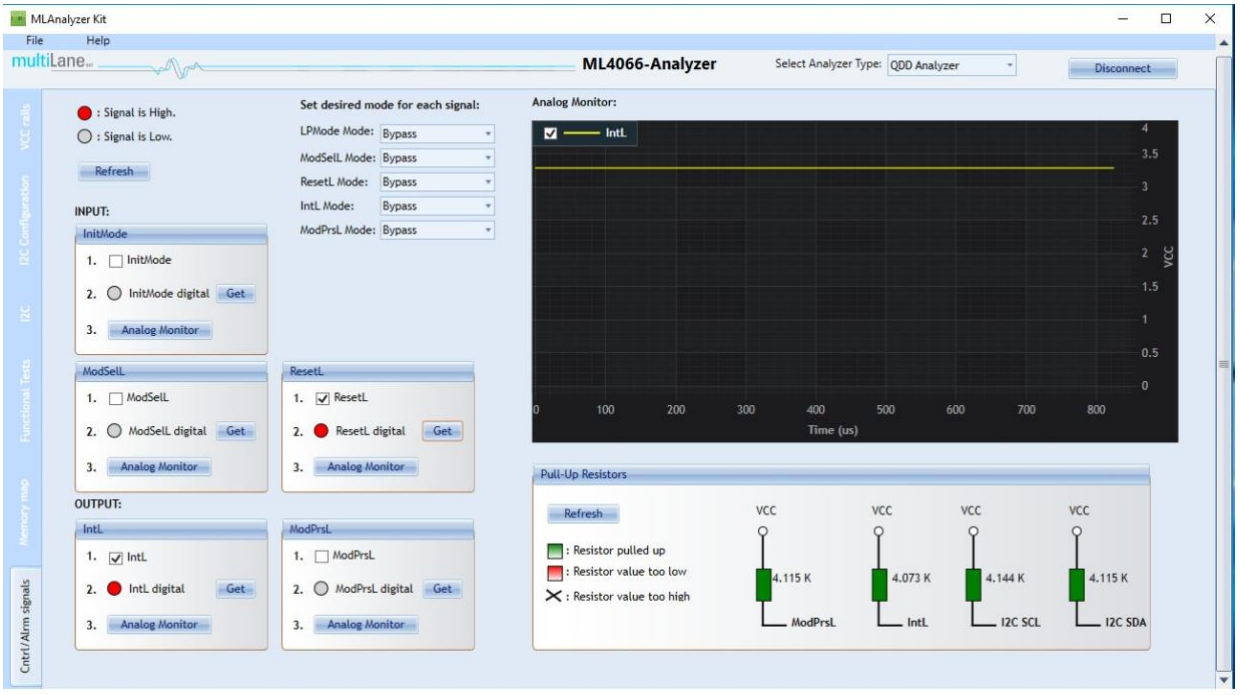


Figure 7: Cntrl/Alrm signals tab

The SFP has different low speed control signals as shown in the figure below.

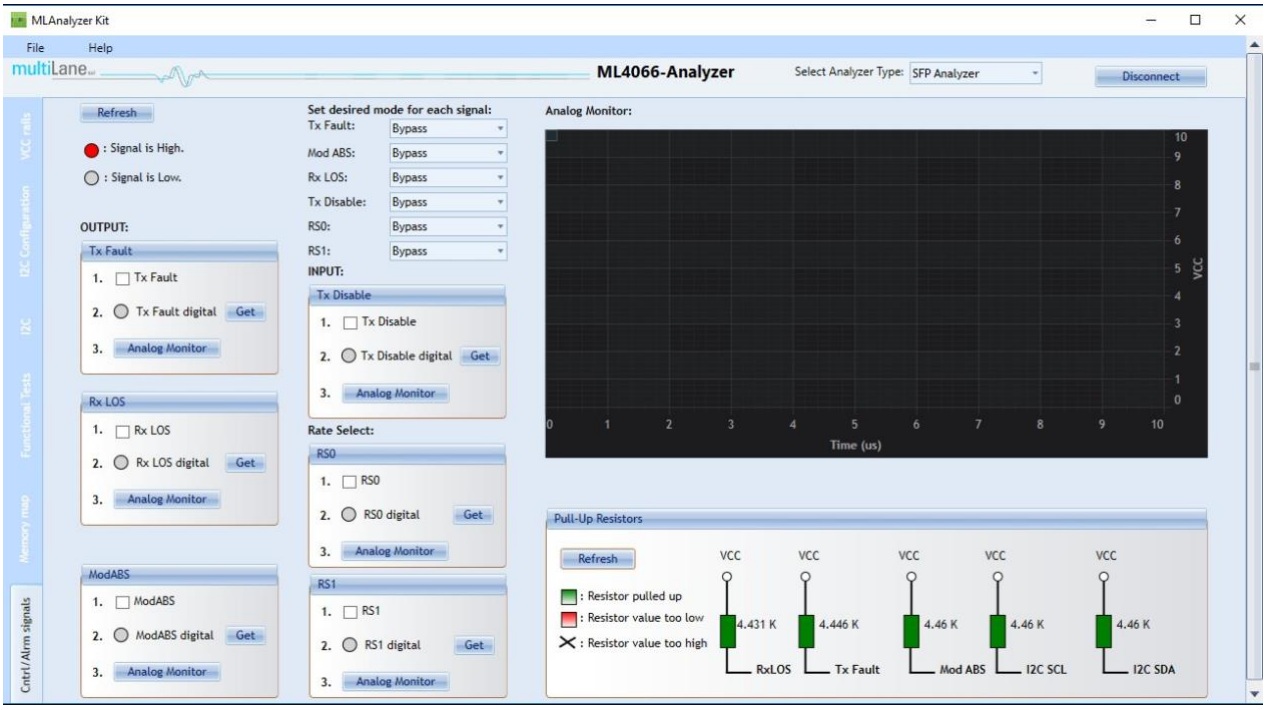


Figure 8- SFP-Analyzer Control signals

2.3 Application Notes

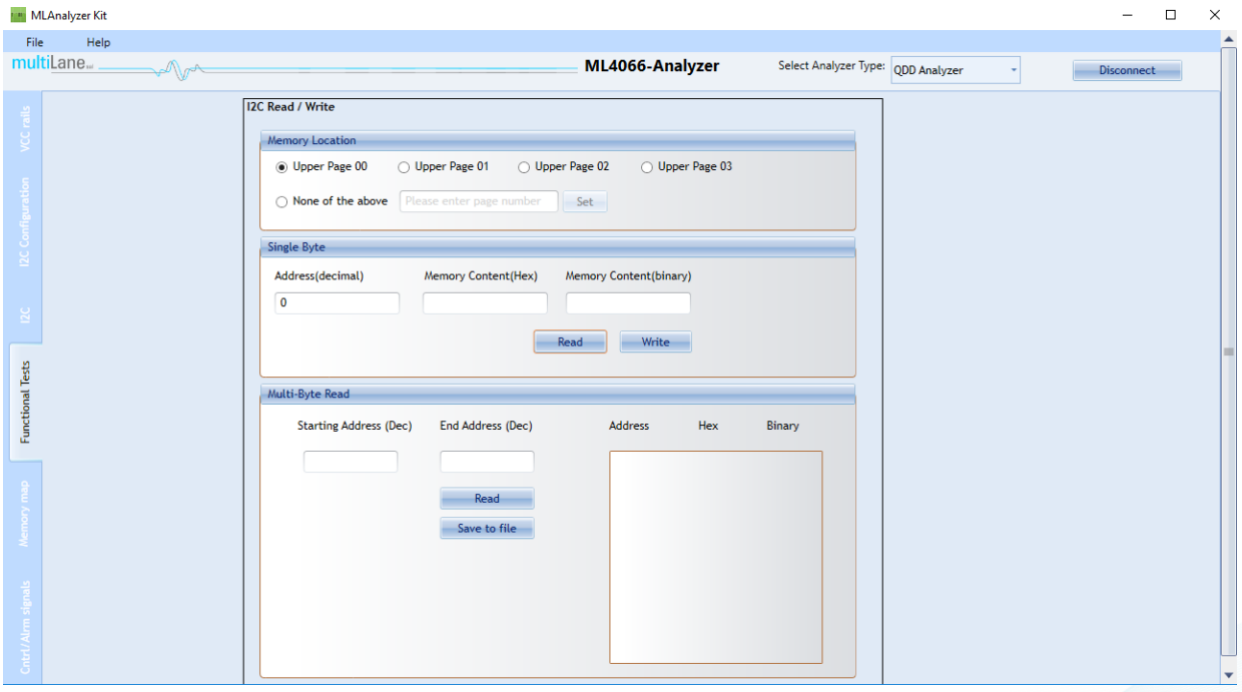
2.3.1 I2C Tab

1. Select “Bypass” mode from the “I2C Configuration” tab
2. In the I2C tab, select the number of samples for the I2C capture, for the I2C read it should be the maximum.
3. Without selecting the “free run” checkbox, click the I2C button to start monitoring, then using your host send an I2C command (read or write) and wait for the I2C Frame Capture.
4. If the “free run” checkbox is selected, the capturing will start immediately after the I2C button is clicked.

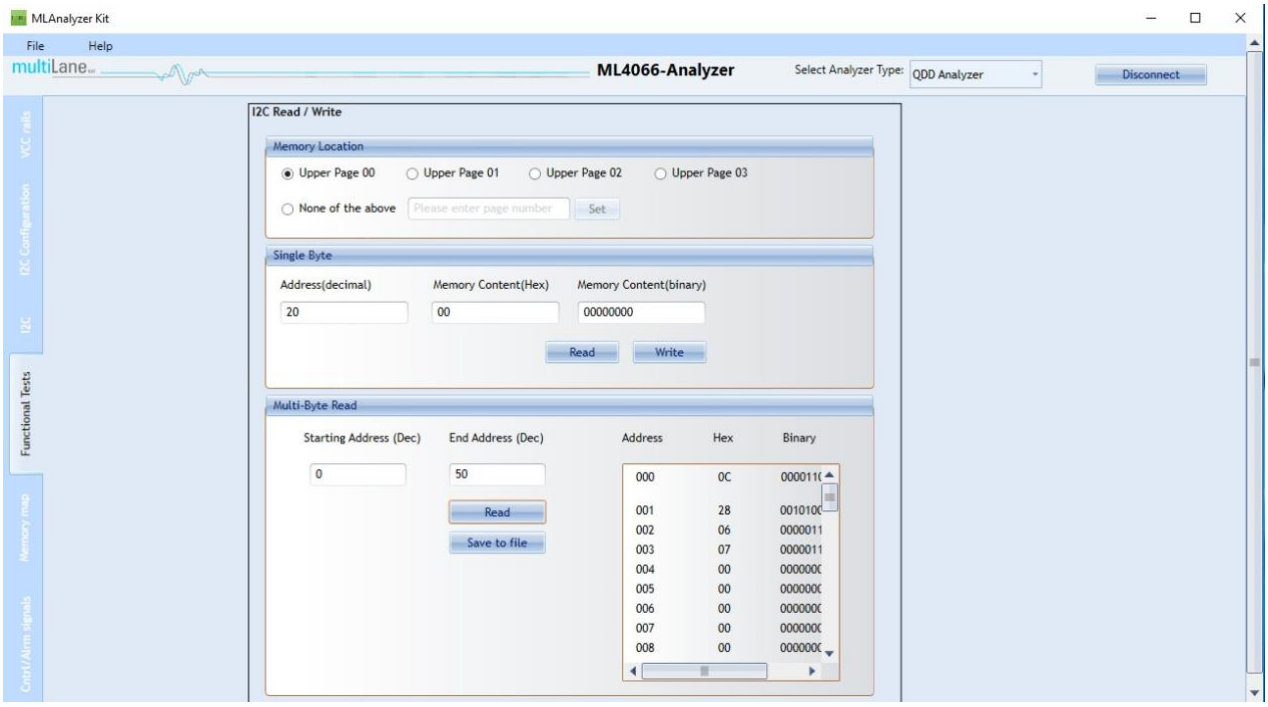
Figure 9: I2C Read

2.3.2 Functional Tests Tab

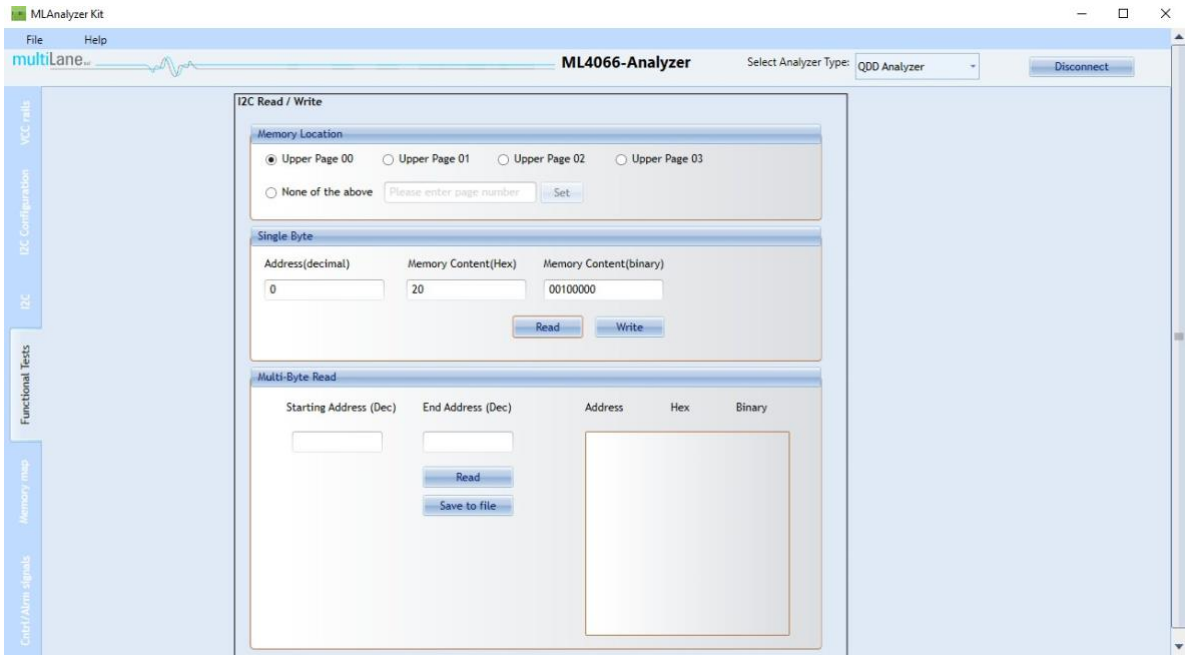
1. Select “Bypass” mode, using your host try to read/write a value from the module. In the Analyzer GUI, the read/write won’t work in this mode because the Host and module communicate directly without the interference of the Analyzer.



2. Select “Internal Master” mode, read address 0 using the Analyzer GUI. This value refers to the one written on the module. The connection between the Host and the Analyzer is cut and using the Host to read will give you FF values.



3. Select “Internal Slave” mode, the reading/writing command from the Analyzer or your Host will give the same value written in the EEPROM.



In the “Memory Map” tab, the grid when clicking “Refresh” displays all data written in the registers and it follows the rules above.

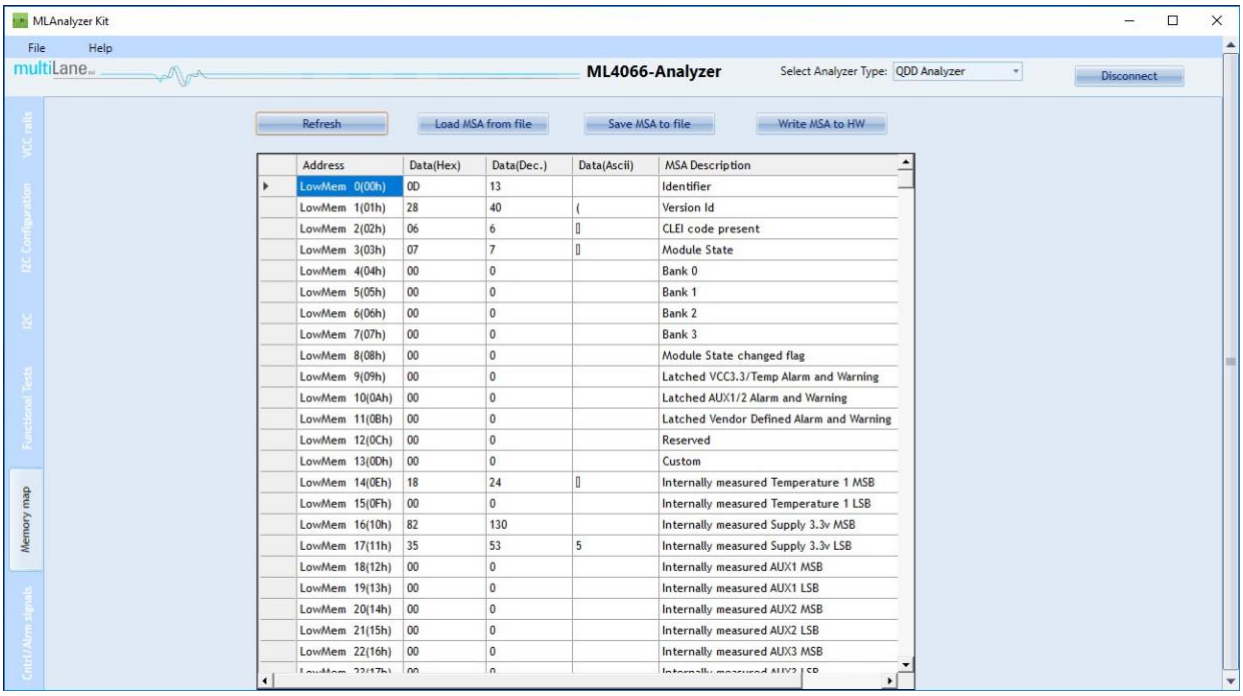
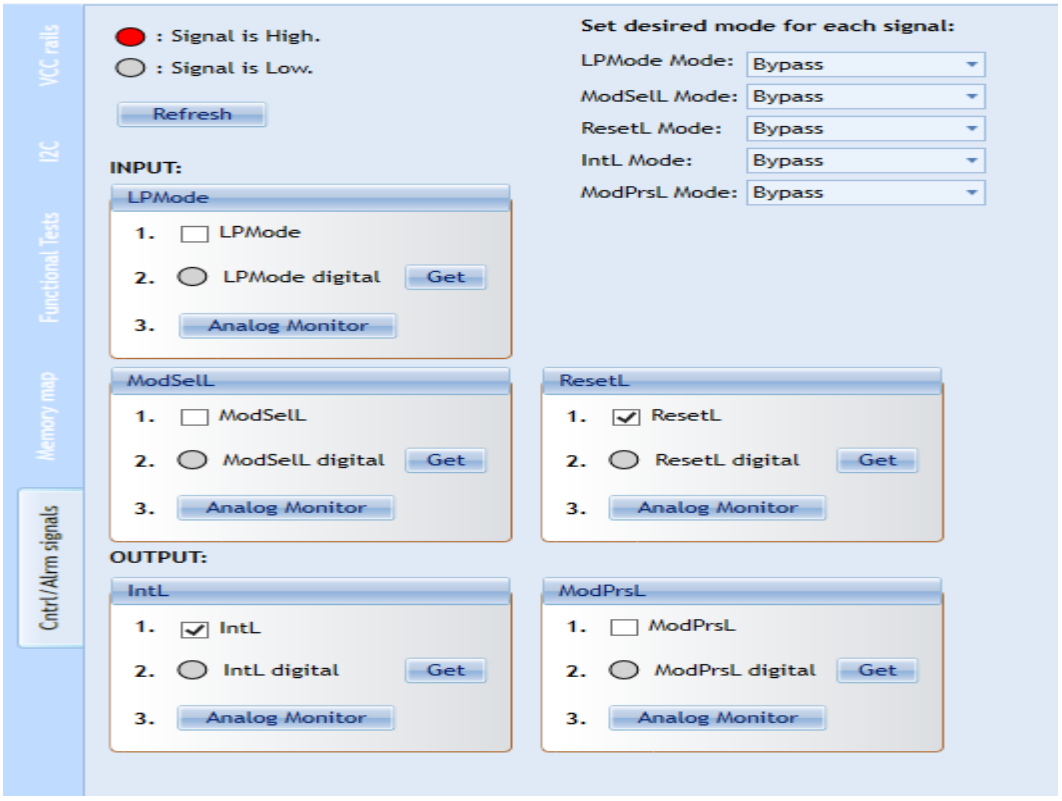


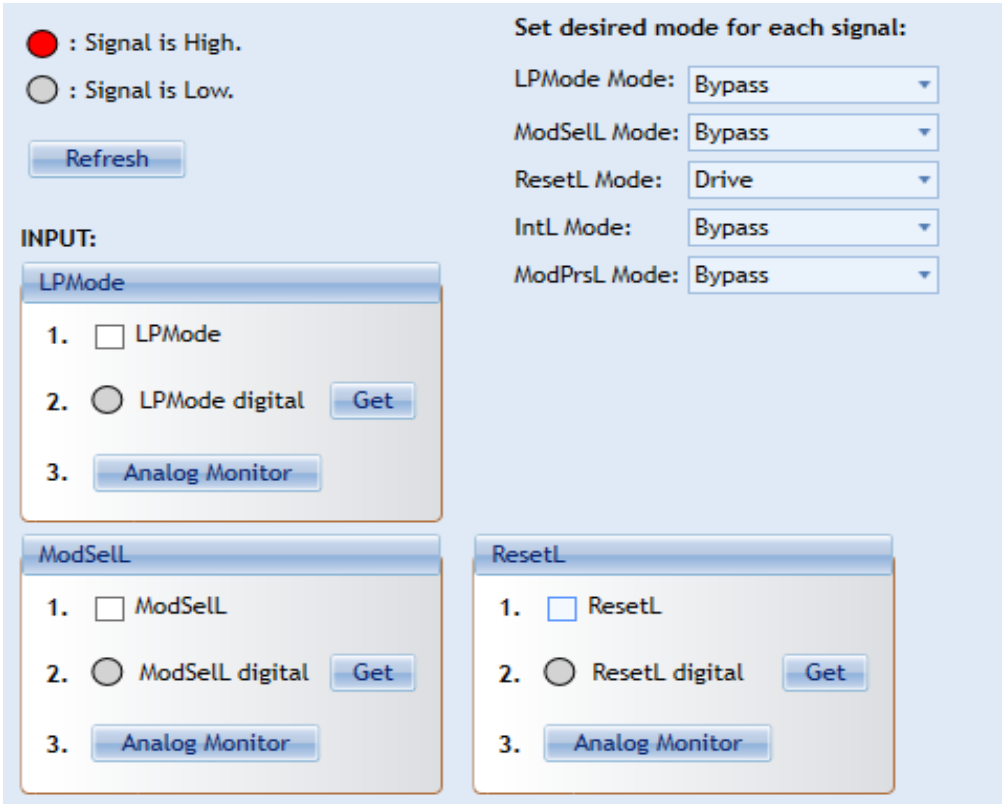
Figure 10: Internal Master

2.3.3 Cntrl/Alrm Tab

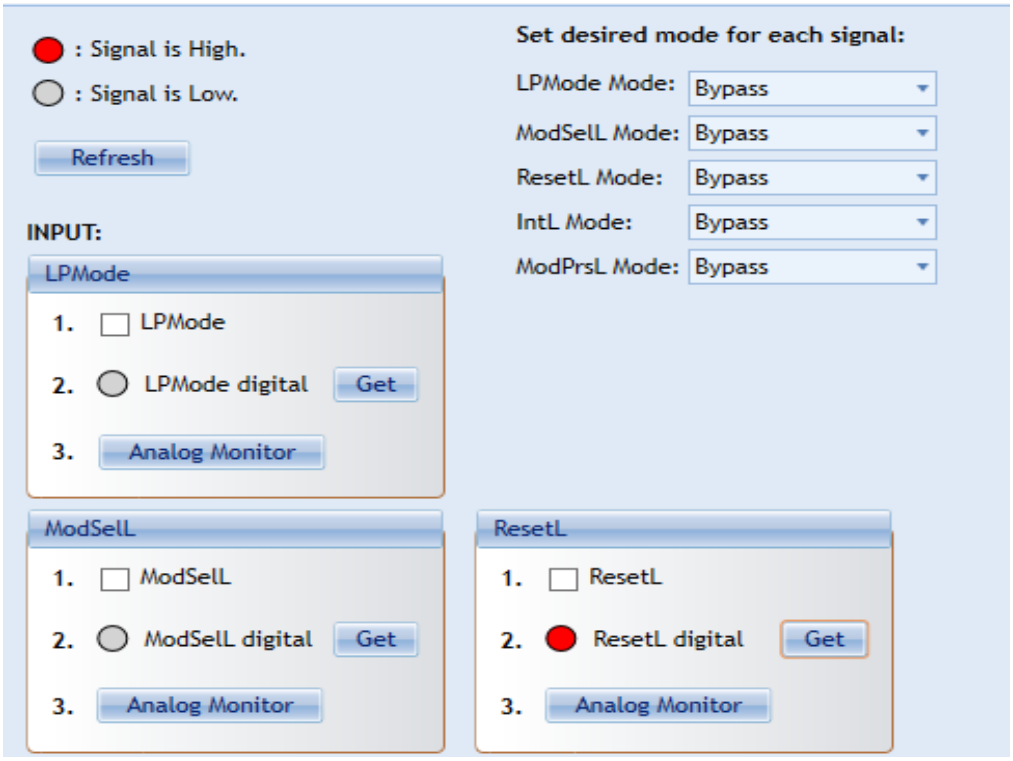
1. The refresh button gets the Status of the signals at the “Drive” mode and the checkboxes reflect its condition.



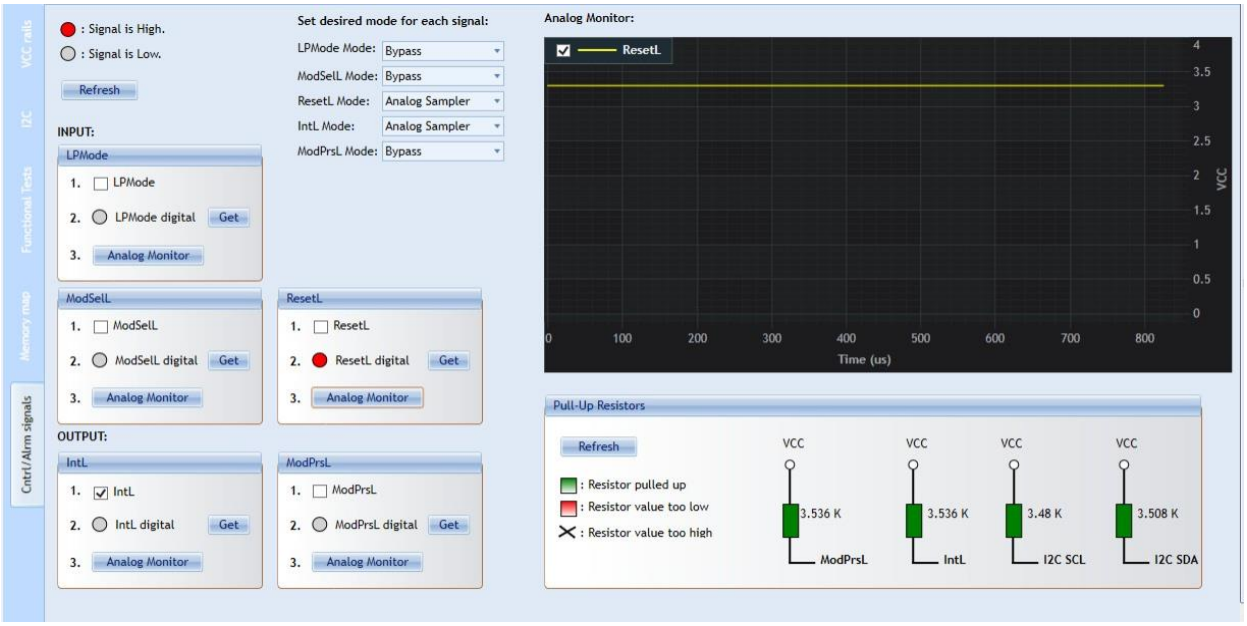
2. Select “Drive” mode for ResetL and toggle the checkbox, the ResetL signal of the module will be activated or deactivated.



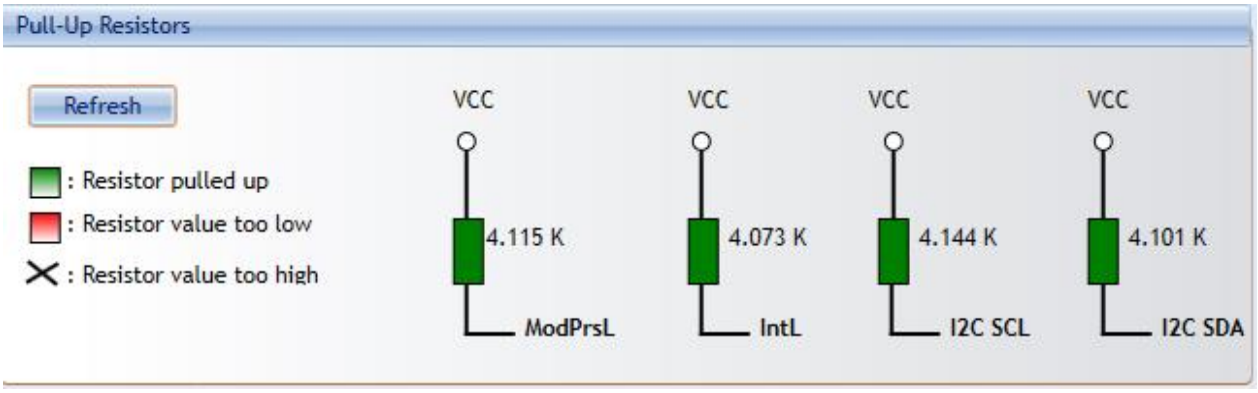
3. Select “Bypass” mode, from you Host try to trigger the ResetL signal. In the analyzer GUI get its status by clicking on “Get” button.



4. Select “Analog Monitor” mode and click on the “Analog Monitor” button of ResetL. The graph displays its DC voltage level from the Host side.



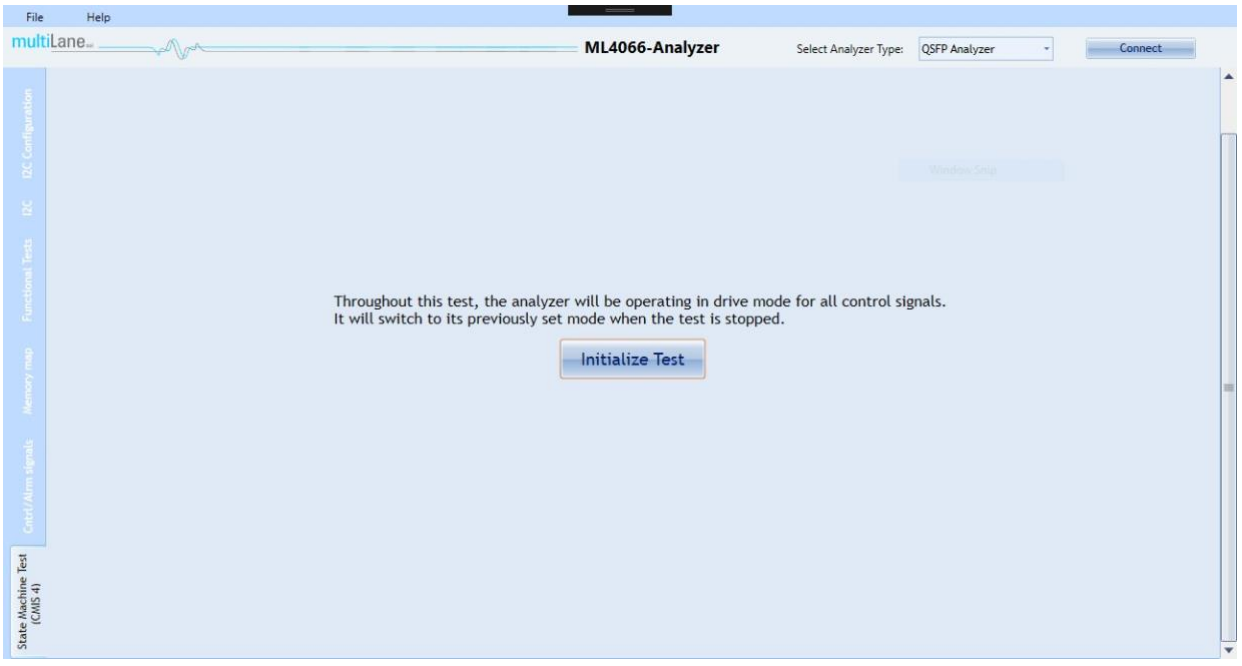
5. In the “Pull-Up Resistors” Groupbox, click “Refresh” button, the values displayed are the values of the pullup resistors at the Host. See section 3.2.5 for more details about the values description.



3. CMIS State Machine Test

This analyzer test works for all QSFP and QDD modules that are **CMIS 4.0** compliant.

The Module State Machine is engaged after module insertion and power on, and thus the test can be started. During the test, different state transitions can be shown and tested by toggling the desired destination state. The Module State Machine is different for devices implementing a paged memory map and those implementing a flat (non-paged) memory map.



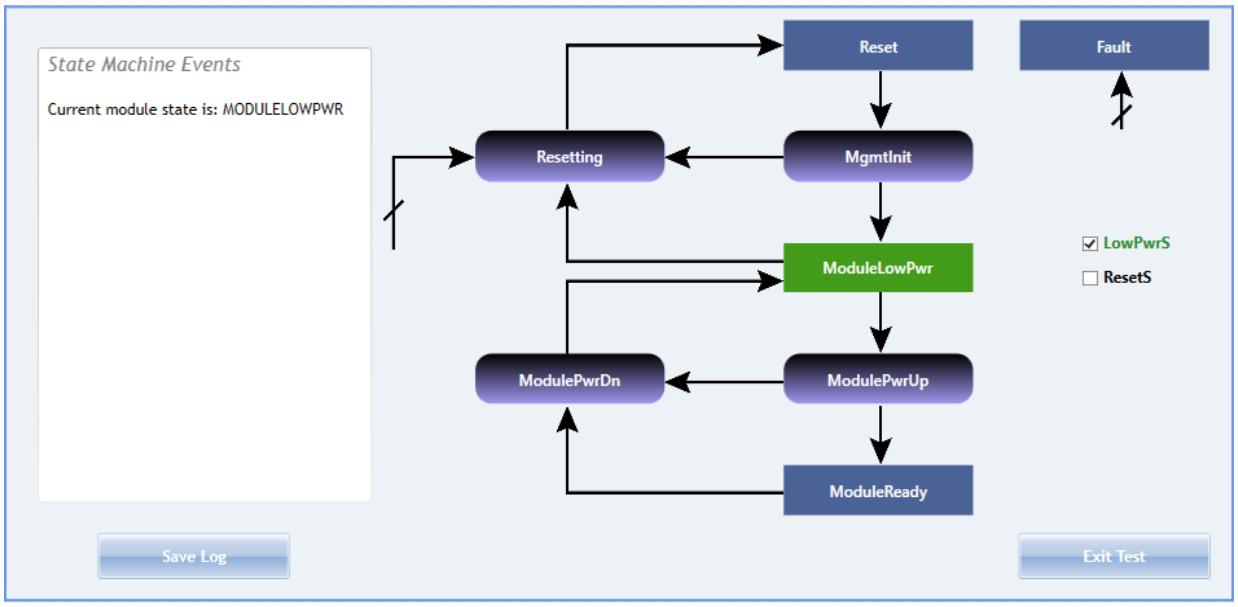
Upon test initialization, the CMIS compliance version is verified and module type is detected. If the latter was not feasible the test would not start normally.

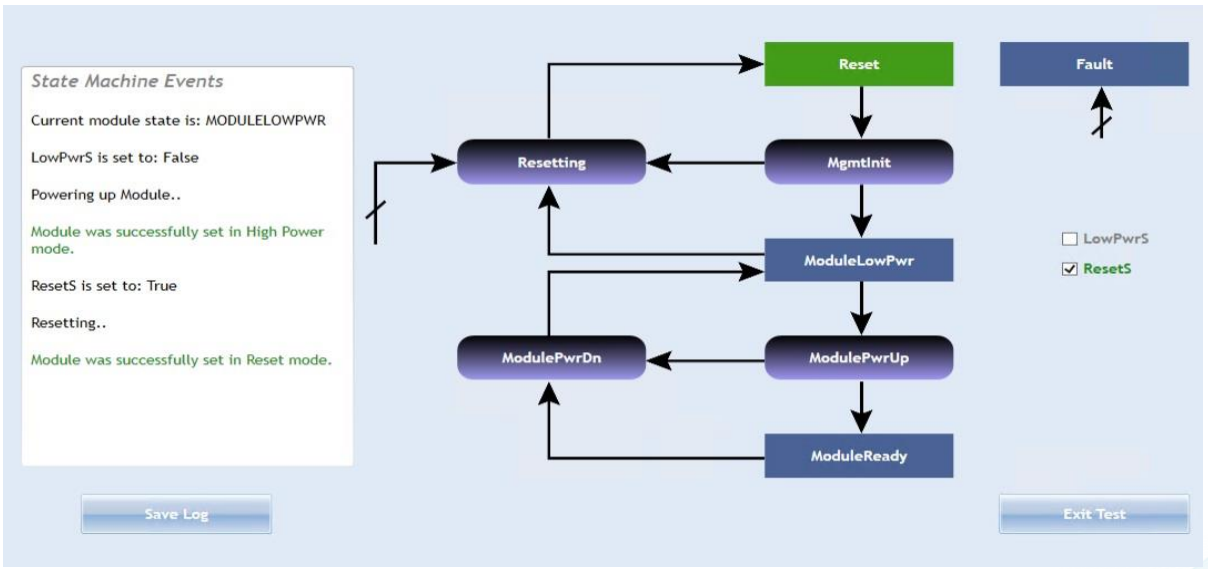
3.1 Paged Memory Modules

If the detected module implements a paged memory map, the below diagram appears showing the current state of the module and the transition signals.

The user can switch to another steady state (Reset, ModuleLowPwr, ModuleReady) by toggling it. State and transition signal changes will appear and events will be logged in the logging box. The logged events can then be saved to a text file possessing the module serial number and the time the test was done.

If an error occurs while transitioning, the module will be thrown into a **Fault** state. This state can be exited only by resetting the module.



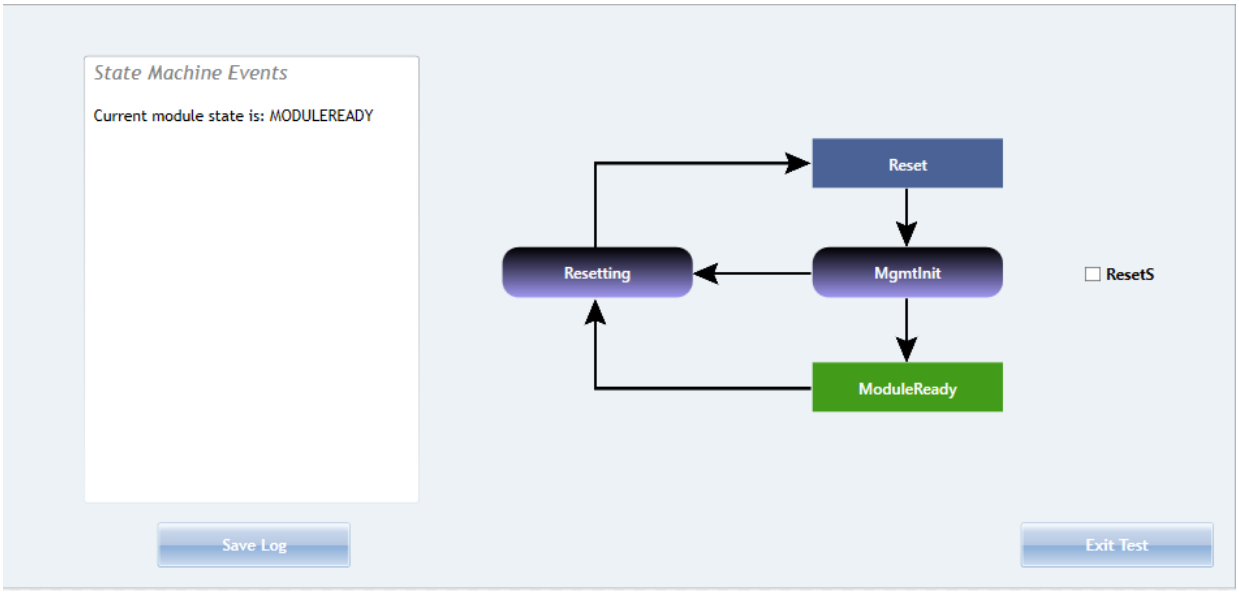


3.2 Flat Memory Modules

If the detected module implements a flat (non-paged) memory map, the below diagram appears showing the current state of the module and the transition signal.

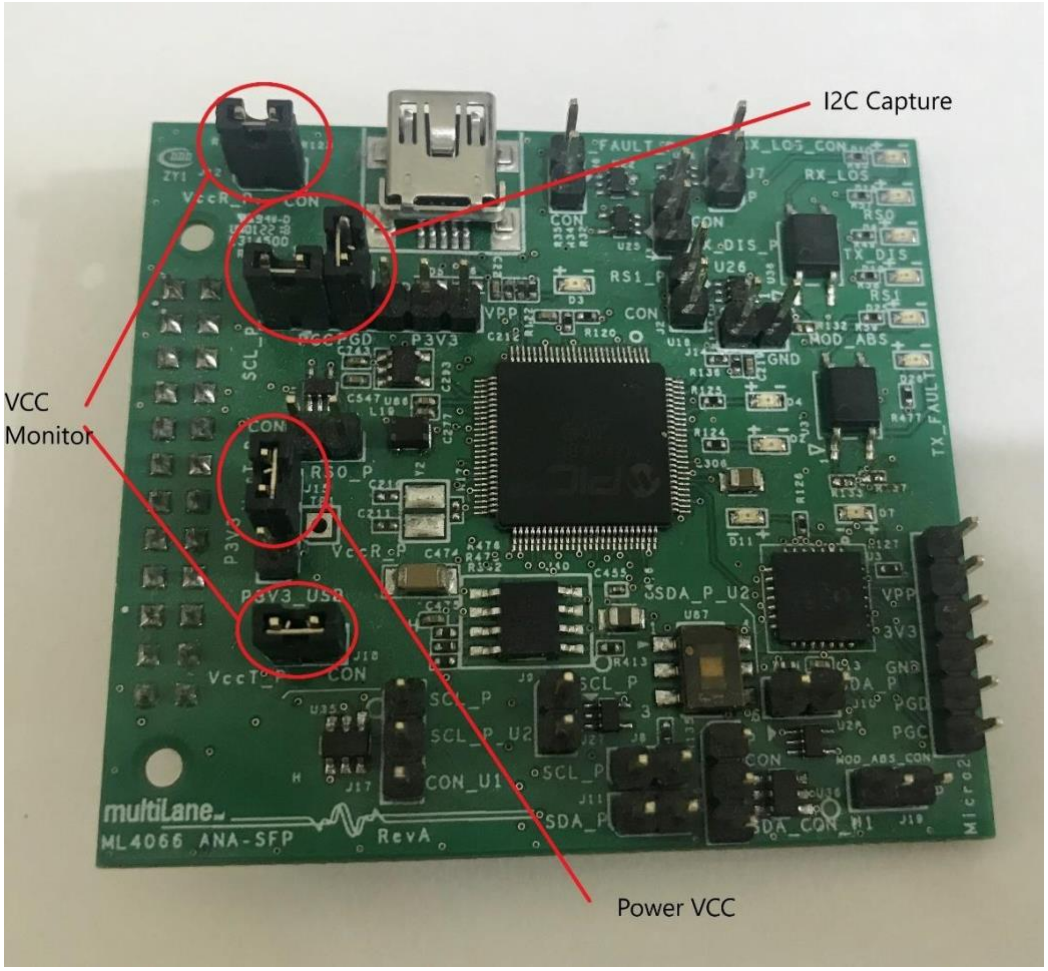
The user can switch between the steady states (Reset or ModuleReady) by toggling any of them. State and transition signal changes will appear and events will be logged in the logging box. The logged events can then be saved to a text file possessing the module serial number and the time the test was done.

If an error occurs while transitioning, the module will be stuck in the transition state until resetting the module or re-initializing the test.



Appendix

- SFP Analyzer jumpers' placement



Revision Information

Revision number	Description	Date
1.0	▪ Preliminary revision	2017/11/27
1.1	▪ Updated parag 3.2 to match version 1.0 of the GUI	2017/12/13
1.2	▪ Adding period selection	2018/1/4
1.3	▪ Adding Resistor pullup and Refresh button in cntrl Tab	2018/4/26
1.4	▪ Adding application notes	2018/5/3
1.5	▪ Update parag 3.3.1	2018/6/4
1.6	▪ Add Appendix	2019/9/4
1.7	▪ Add CMIS 4.0 State Machine Test	2020/3/2

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